Investigating SRAM PUFs in large CPUs and GPUs

Or: “Can’t we just rewrite the BIOS?”

SPACE 2015, MNIT, Jaipur, India

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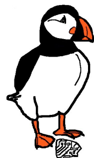
PUFFIN project



"The Physically unclonable functions found in standard PC components (PUFFIN) project intends to study and show the existence of SRAM PUFs and other types of PUFs in standard PCs, laptops, mobile phones and consumer electronics."
— http://puffin.eu.org/

Outline

Introduction to PUFs

CPUs

GPUs

Conclusions

Physically Unclonable Functions

PUFs:

Physically Unclonable Functions

PUFs:

- physical

Physically Unclonable Functions

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- easy to evaluate

Physically Unclonable Functions

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Physically Unclonable Functions

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Emergent behaviour through random physical variations.

Sources of PUFs

Inside ICs:

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- signal delay variations
  - ring oscillators
  - multiplexers

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- interaction between cross-coupled cells
  - SRAM
  - flip-flops
  - latches

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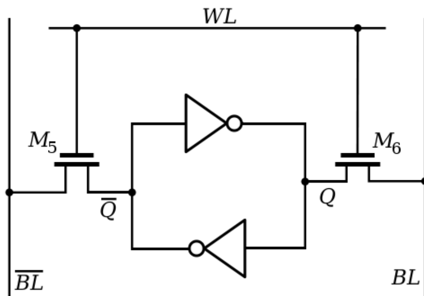

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- signal delay variations
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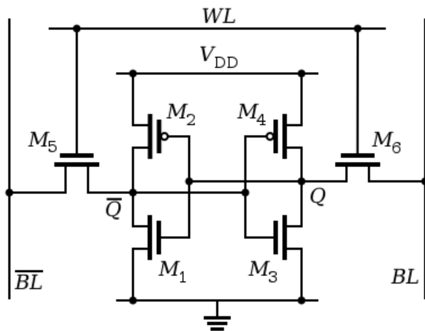

Sources of PUFs

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- magnetism (magstripe)

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Sources of PUFs

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Typically found in specially designed hardware components

SRAM PUFs

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- Microscopic differences determine likelihood of power-up state

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- Many cells are stable across reboots
  - Unique identification of electric components
  - Protect against counterfeiting
  - Device-unique “fingerprint” as a root of trust

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- But not all; provides true randomness
  - Input for a CSRNG

SRAM PUFs

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  - Unique identification of electric components
  - Protect against counterfeiting
  - Device-unique "fingerprint" as a root of trust
- But not all; provides true randomness
  - Input for a CSRNG
- Already present in many devices as uninitialized memory

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Targets

Modern, common, consumer-grade AMD64 CPUs:

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- AMD
- Intel

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High probability of SRAM used for registers and cache

Registers

AMD64 has many registers:

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- 16 64-bit General-Purpose (GP) registers

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- Stuff like conditional registers, floating point / MMX ...

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Easy to reach

Caches

Modern AMD64 CPUs have multiple layers of cache

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- Transparent window into RAM
- AMD64 memory setup is complicated

Caches

Modern AMD64 CPUs have multiple layers of cache

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Hard to reach

Security features

But CPUs evolved with security features:

- virtual memory
- address space separation
- memory protection

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So can we actually read out uninitialized SRAM?

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But CPUs evolved with security features:

- virtual memory
- address space separation
- memory protection

So can we actually read out uninitialized SRAM?

Well, maybe before the OS is really running?

AMD64 boot (somewhat simplified)

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1. Power on

AMD64 boot (somewhat simplified)

1. Power on
2. BIOS starts

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1. Power on
2. BIOS starts
3. ???

AMD64 boot (somewhat simplified)

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4. Profit

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If we can avoid the ??? and move directly to profit:

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If we can avoid the ??? and move directly to profit:

- widely deployable

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If we can avoid the ??? and move directly to profit:

- widely deployable
- compatible with a lot of hardware

AMD64 boot (somewhat simplified)

1. Power on
2. BIOS starts
3. ???
4. Profit

If we can avoid the ??? and move directly to profit:

- widely deployable
- compatible with a lot of hardware
- least amount of effort

Uninitialized state access

Requirements:

Uninitialized state access

Requirements:

- Early

Uninitialized state access

Requirements:

- Early
- Readable

Uninitialized state access

Requirements:

- Early
- Readable
- Editable

Kernel patching

So you patch the Linux kernel:

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Unfortunately, “that memory” was zeroes and e.g.

- EFI_STATUS_CODE_SPECIFIC_DATA_GUID
- EFI_PROCESSOR_PRODUCER_GUID

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- read that memory with a kernel module at a later point

Unfortunately, "that memory" was zeroes and e.g.

- EFI_STATUS_CODE_SPECIFIC_DATA_GUID
- EFI_PROCESSOR_PRODUCER_GUID

So XMM-registers were modified before the kernel started

Power-on state access

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Well, maybe early in the bootloader?

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5. Run main BIOS / UEFI payload

AMD64 boot (simplified)

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5. Run main BIOS / UEFI payload
6. Find bootable devices

AMD64 boot (simplified)

1. Power on
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3. Initialize firmware
4. Put CPU in correct mode
5. Run main BIOS / UEFI payload
6. Find bootable devices
7. Run bootsector code

AMD64 boot (simplified)

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8. More initialization and OS loading

AMD64 boot (simplified)

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3. Initialize firmware
4. Put CPU in correct mode
5. Run main BIOS / UEFI payload
6. Find bootable devices
7. Run bootsector code
8. More initialization and OS loading
9. Run OS kernel

GRUB

GRand Unified Bootloader

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- Installable on disk (easy edits)

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- Open source

Method

Take some random old Intel machine

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1. Install linux

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2. Install vanilla grub

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1. Install linux
2. Install vanilla grub
3. Clone GRUB

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4. Until registers are read:
   a. Figure out how GRUB works internally

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Take some random old Intel machine

1. Install linux
2. Install vanilla grub
3. Clone GRUB
4. Until registers are read:
    a. Figure out how GRUB works internally
    b. Edit GRUB

Method

Take some random old Intel machine

1. Install linux
2. Install vanilla grub
3. Clone GRUB
4. Until registers are read:
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   b. Edit GRUB
   c. Compile GRUB

Method

Take some random old Intel machine

1. Install linux
2. Install vanilla grub
3. Clone GRUB
4. Until registers are read:
    a. Figure out how GRUB works internally
    b. Edit GRUB
    c. Compile GRUB
    d. Install GRUB

Method

Take some random old Intel machine

1. Install linux
2. Install vanilla grub
3. Clone GRUB
4. Until registers are read:
    a. Figure out how GRUB works internally
    b. Edit GRUB
    c. Compile GRUB
    d. Install GRUB
    e. Reboot

Method

Take some random old Intel machine

1. Install linux
2. Install vanilla grub
3. Clone GRUB
4. Until registers are read:
    a. Figure out how GRUB works internally
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    f. Pray

Method

Take some random old Intel machine

1. Install linux
2. Install vanilla grub
3. Clone GRUB
4. Until registers are read:
   a. Figure out how GRUB works internally
   b. Edit GRUB
   c. Compile GRUB
   d. Install GRUB
   e. Reboot
   f. Pray
   g. If praying fails: boot from install media and GOTO 2

GRUB internals

1. GRUB starts

GRUB internals

1. GRUB starts
2. Some machine initialization

GRUB internals

1. GRUB starts
2. Some machine initialization
3. Terminal initialization

GRUB internals

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4. Load modules

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GRUB internals

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2. Some machine initialization
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Doesn't seem to touch XMM-registers

GRUB internals, edited

1. GRUB starts
2. Some machine initialization
3. Terminal initialization
4. Read and dump XMM-registers to console
5. Load modules
6. Display boot menu
7. . . .

Reading registers from within GRUB

1. Allocate some memory

Reading registers from within GRUB

1. Allocate some memory
2. Fill with a known pattern

Reading registers from within GRUB

1. Allocate some memory
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3. Use some ASM to copy each register

Reading registers from within GRUB

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2. Fill with a known pattern
3. Use some ASM to copy each register
4. Dump memory to console

Reading registers from within GRUB

1. Allocate some memory
2. Fill with a known pattern
3. Use some ASM to copy each register
4. Dump memory to console
5. Sleep 60 seconds

Reading registers from within GRUB

1. Allocate some memory
2. Fill with a known pattern
3. Use some ASM to copy each register
4. Dump memory to console
5. Sleep 60 seconds while PhD-student writes furiously

Some gotchas

1. Allocate some memory
2. Fill with a known pattern
3. Explicitly set CPU in protected mode
4. Fix some other preconditions for SSE-instructions
5. Use some ASM to copy each register
6. Dump memory to console
7. Sleep 60 seconds while PhD-student writes furiously

Success! (Abort, retry, fail?)

XMM0: Some static data persisent over boots
XMM1–7: 0

Google

- XMM0 turns out to contain some CPUID-stuff
- Found in source files of the Coreboot project
- Likely explanation: BIOS uses XMM-registers

Power-on state access

Requirements:

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- Editable

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So can we actually read out uninitialized SRAM?

Power-on state access

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- Readable
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So can we actually read out uninitialized SRAM?

Okay, okay, can't we just rewrite the BIOS?

AMD64 boot (simplified further)

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BIOS

BIOS is as early as you can get

BIOS

BIOS is as early as you can get
BIOS is not:

- Readable
- Editable

Coreboot

Formerly linuxBIOS

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But:

- Each board booted by coreboot requires explicit support

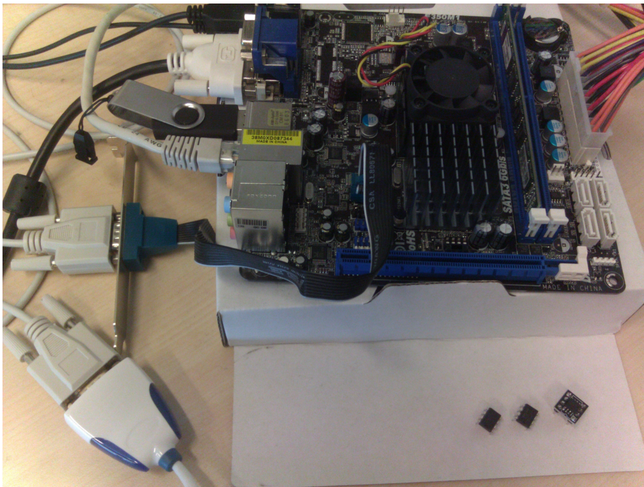
Not general

Port it ourselves or buy a supported board
Requirements:

1. Recent CPU
2. AMD or Intel
3. Relatively cheap
4. *Socketed* BIOS chip

ASROCK e350m1 w/ AMD e350 APU (CPU + Northbridge + stuff)
Some compatible BIOS chips

ASROCK e350m1



Method

Target registers first

1. Install linux
2. Clone coreboot
3. Get vanilla coreboot running on the board

Intermezzo: “compatible” chips aren’t

Clock speed “bug” in coreboot: BIOS chips incompatible
(I blame the chip vendor, not coreboot devs)
Last-minute trip to FOSDEM to exchange chips with coreboot devs

Method

Figure out how coreboot works

- Actually quite complex for something so limited in scope

AMD64 boot (simplified less)

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AMD64 boot (simplified less)

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4. Put CPU in protected mode
5. Do some CPU initialization

AMD64 boot (simplified less)

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6. Initialize cache-as-ram for stack-based computing

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7. Initialize Super-IO

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5. Do some CPU initialization
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7. Initialize Super-IO
8. Start outputting over serial port

AMD64 boot (simplified less)

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9. ...

AMD64 boot (simplified less)

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2. Load BIOS ROM from NVRAM
3. Jump to address 0xFFF0
4. Put CPU in protected mode
5. Do some CPU initialization
6. Initialize cache-as-ram for stack-based computing
7. Store XMM-registers in memory
8. Initialize Super-IO
9. Start outputting over serial port
10. Dump XMM-registers to serial port
11. ...

Success! (Abort, retry, fail?)

XMM0–7: 0

But: manual analysis of coreboot disasm: xmm2-xmm7 are untouched before patch code path.

The importance of documentation

"Table 14-1 shows the initial processor state following either RESET or INIT. Except as indicated, processor resources generally are set to the same value after either RESET or INIT."

"SSE State XMM0–XMM15 = 0"

"Upon power-on reset, all 16 YMM/XMM registers are cleared to +0.0. However, initialization by means of the #INIT external input signal does not change the state of the YMM/XMM registers."

"Following a RESET (but not an INIT), all instruction and data caches are disabled, and their contents are invalidated (the MOESI state is set to the invalid state)."

Dead end?

They implement what they say in the documentation (unfortunately)

Dead end?

They implement what they say in the documentation (unfortunately)

Or do they?

Close examination of cache-as-ram initialization: explicit zeroing of allocated stack

AMD64 boot (simplified less)

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4. Put CPU in protected mode
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    a. Fix preconditions for cache-as-ram
    b. Allocate stack
    c. Ensure stack is not zeroed

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5. Do some CPU initialization
6. Initialize cache-as-ram for stack-based computing
    a. Fix preconditions for cache-as-ram
    b. Allocate stack
    c. Ensure stack is not zeroed
7. Initialize Super-IO
8. Start outputting over serial port
9. Dump entire stack to serial port

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   a. Fix preconditions for cache-as-ram
   b. Allocate stack
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7. Initialize Super-IO
8. Start outputting over serial port
9. Dump entire stack to serial port
10. ...

Fail

Everything except some space used for function calls is 0

Fail

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So can we actually read out uninitialized SRAM?

Fail

Everything except some space used for function calls is 0

So can we actually read out uninitialized SRAM?

No.

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Security features?

No protection like the CPUs

Targets

Modern, common, consumer-grade Nvidia GPUs: Nvidia GTX 295

- Two GPU devices per card, with
- 30 multiprocessors per device, with
- 16384 32-bit registers, and
- 16KiB shared memory

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Modern, common, consumer-grade Nvidia GPUs: Nvidia GTX 295

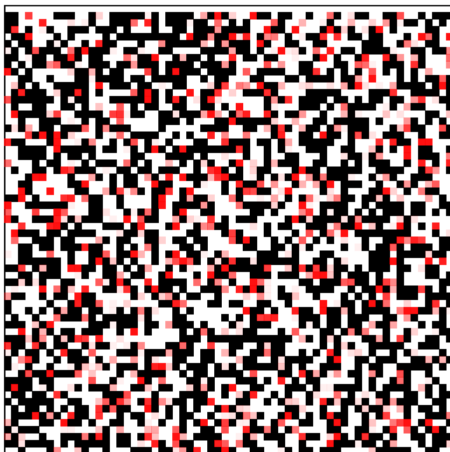
- Two GPU devices per card, with
- 30 multiprocessors per device, with
- 16384 32-bit registers, and
- 16KiB shared memory

High probability of SRAM used for registers and shared memory

Shared memory

- Easier to access than the registers
- We were able to read 490KiB of shared memory in each GPU, and repeated that on 17 devices
- Nice PUF properties
- No obstacles to building PUFs on these devices

Measurements / probabilities



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Difficulties

- Decompiling and analyzing flow of BIOS code
- Compilers using XMM-registers as scratch-registers
- Ensuring negative results are not caused by human error
- Complexity of bringing up an AMD64 machine

Code

Available at
https://www.polvanaubel.com/research/puf/x86-64/code/[1]

[1] Actually, http://www.polvanaubel.com/research/puf/x86-64/code/ until I get a chance to fix it.